

Henrik Forstén

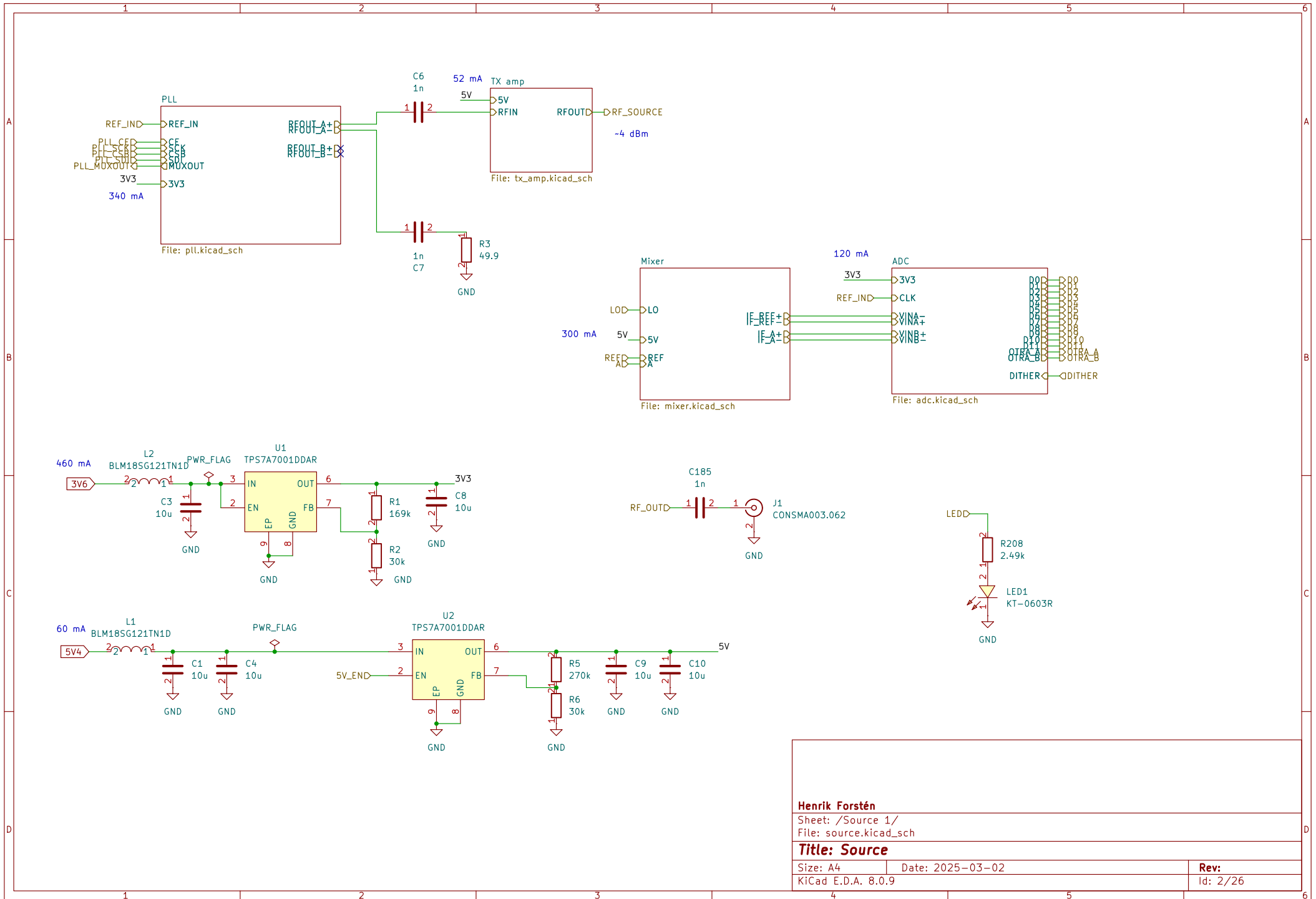
Sheet: /
File: vna3.kicad_sch

Title: Top

Size: A4 Date: 2025-03-02

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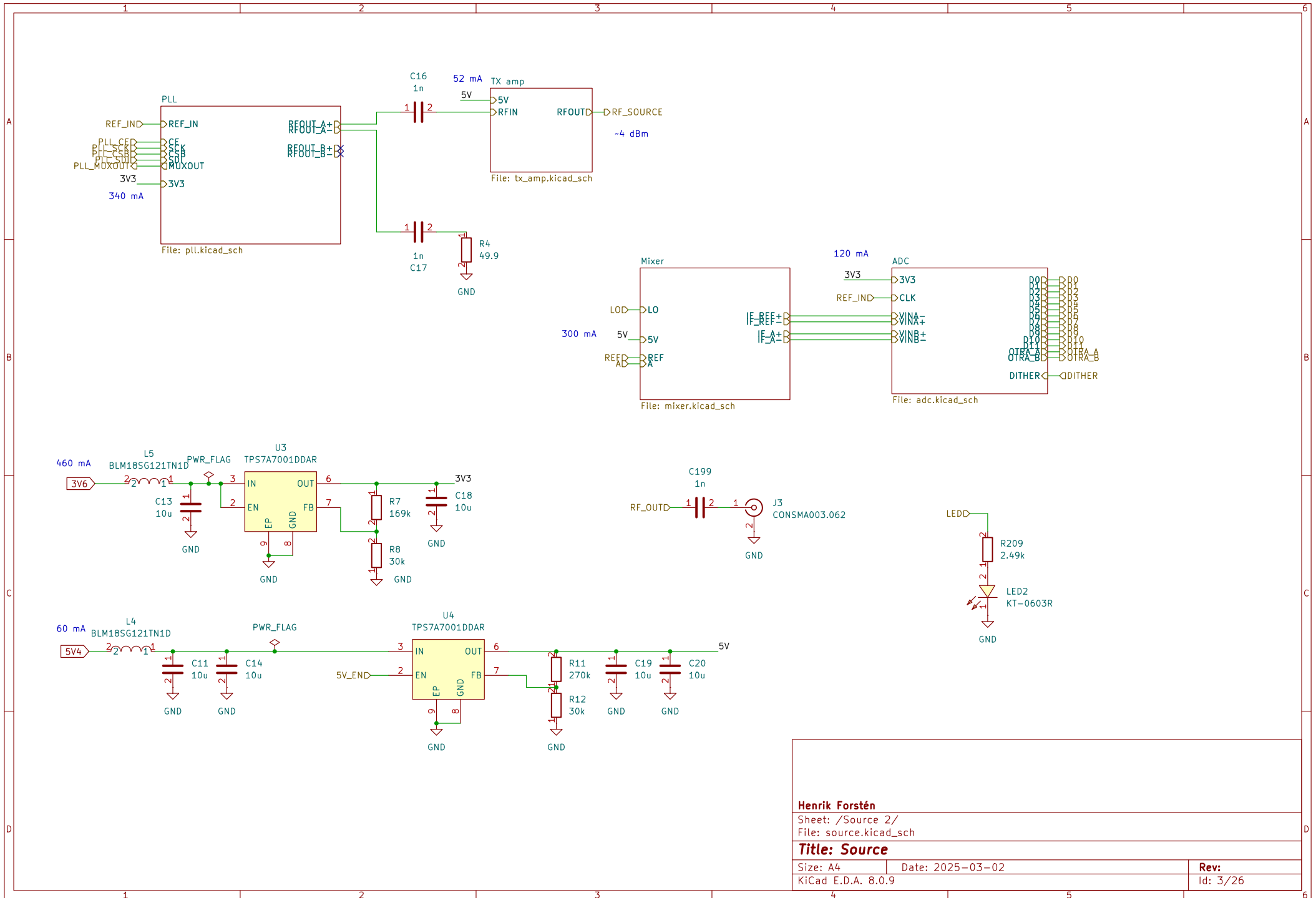
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Sheet: /Source 1/
File: source.kicad_sch

Title: Source

Size: A4 Date: 2025-03-02
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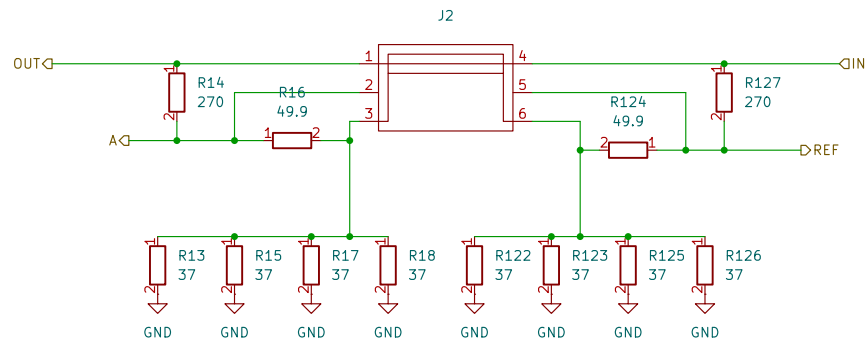
Henrik Forstén

Sheet: /Source 2/
File: source.kicad_sch

Title: Source

Size: A4 Date: 2025-03-02
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Sheet: /Coupler1/
File: coupler.kicad_sch

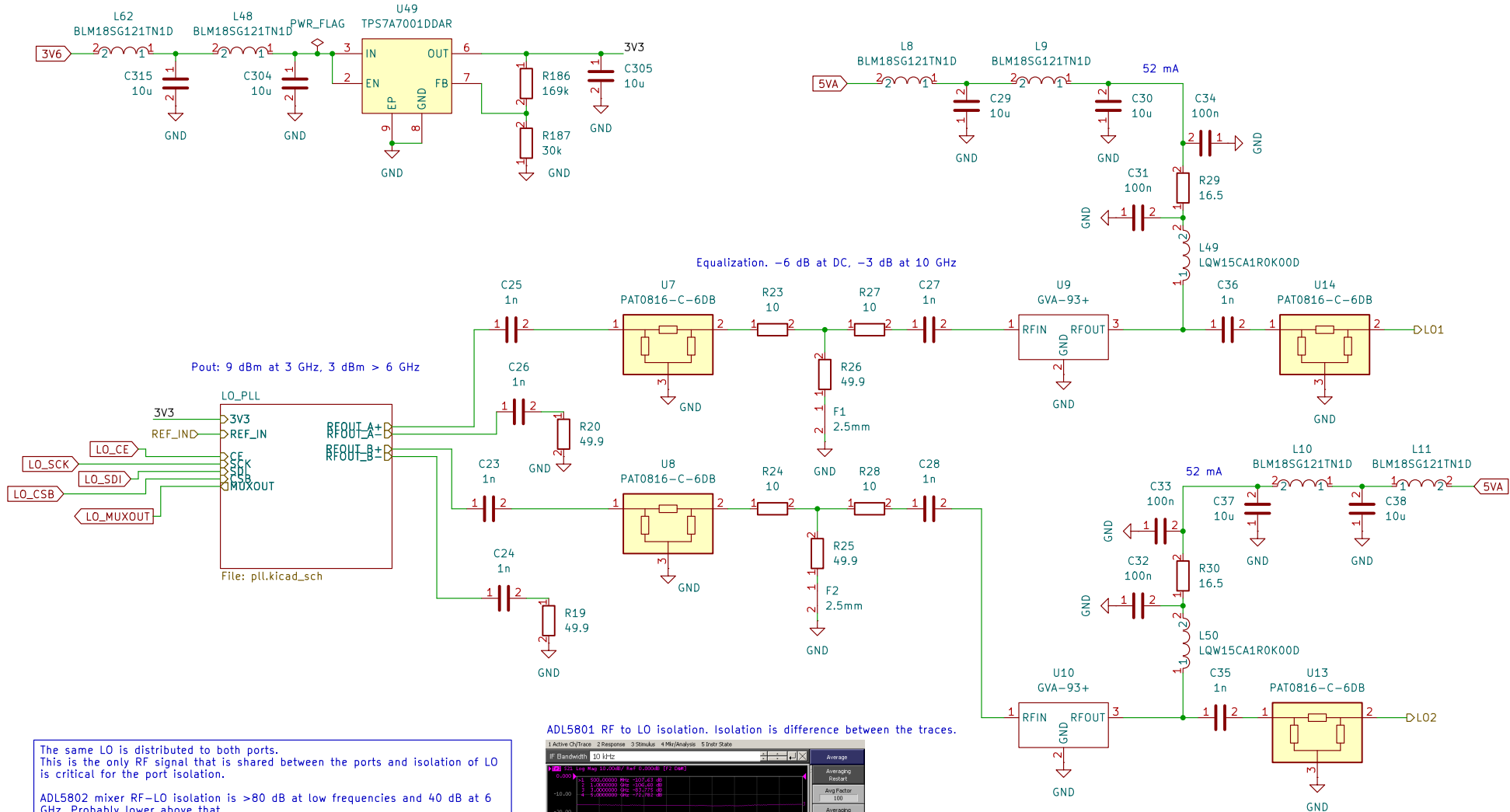
Title: Coupler

Size: A4 Date: 2025-03-02

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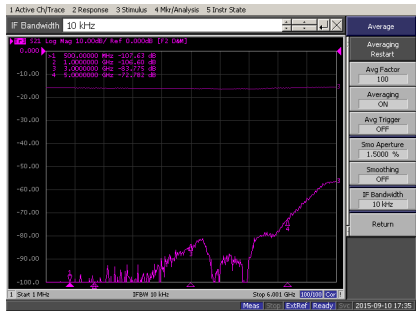
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Pout: 9 dBm at 3 GHz, 3 dBm > 6 GHz

Equalization, -6 dB at DC, -3 dB at 10 GHz

ADL5801 RF to LO isolation. Isolation is difference between the traces.



The same LO is distributed to both ports. This is the only RF signal that is shared between the ports and isolation of LO is critical for the port isolation.

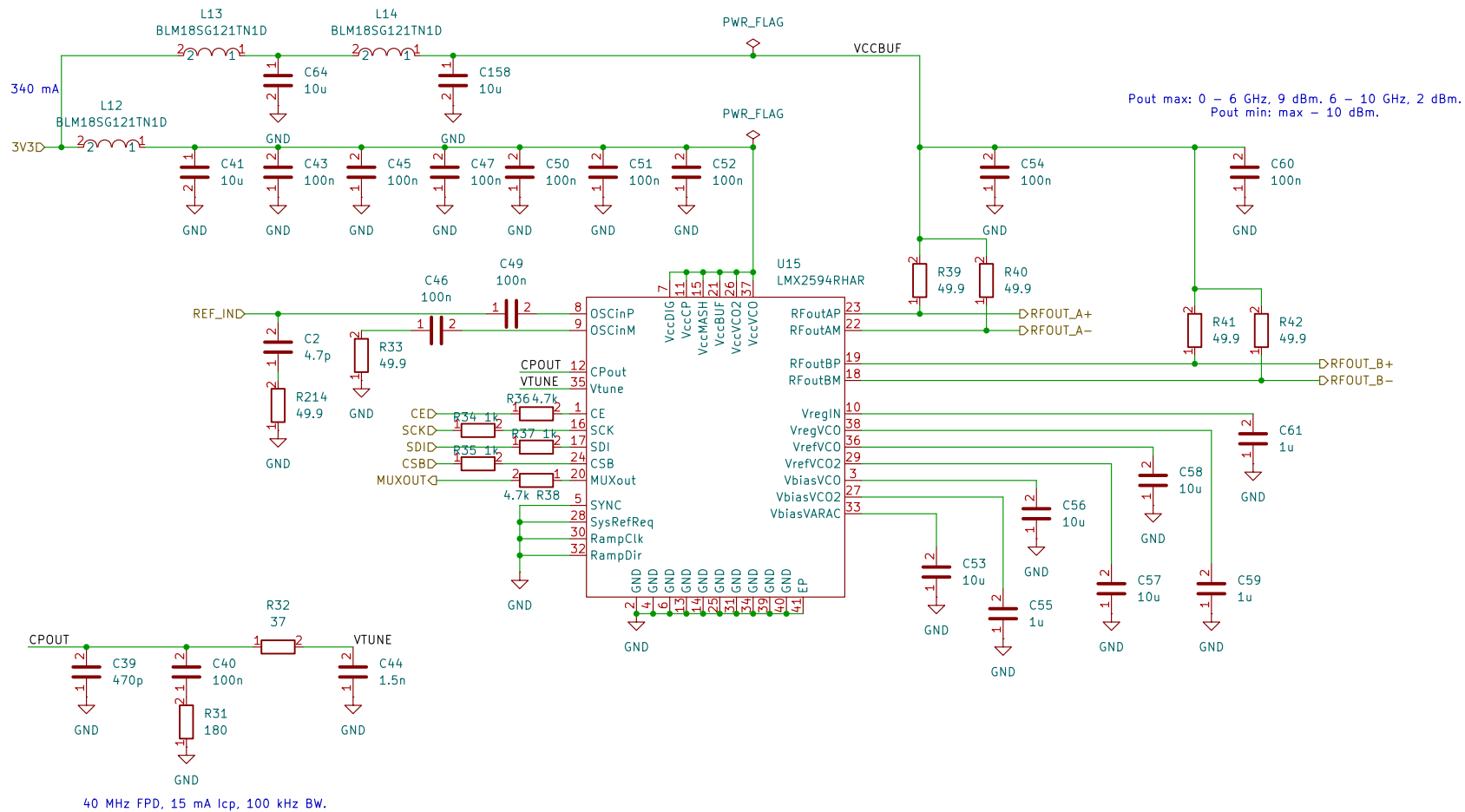
ADL5802 mixer RF-LO isolation is >80 dB at low frequencies and 40 dB at 6 GHz. Probably lower above that. (<https://ez.analog.com/rf/f/q-a/74082/adl5801-rf-to-lo-isolation>)

For >100 dB port isolation LO path needs at least 60 dB isolation in LO path.

LMX2594 is quoted to have 50 dB port to port isolation, but this is from internal VCO to output port. Output to output isolation could be better, but in the worst case it's about the same. Due to layout and output trace coupling it could be even worse at high frequencies.

Adding amplifiers and attenuators adds isolation to LO path.

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Sheet: /LO/	
File: lo.kicad_sch	
Title: LO	
Size: A4	Date: 2025-03-02
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Sheet: /LO/LO_PLL/

File: pll.kicad_sch

Title: PLL

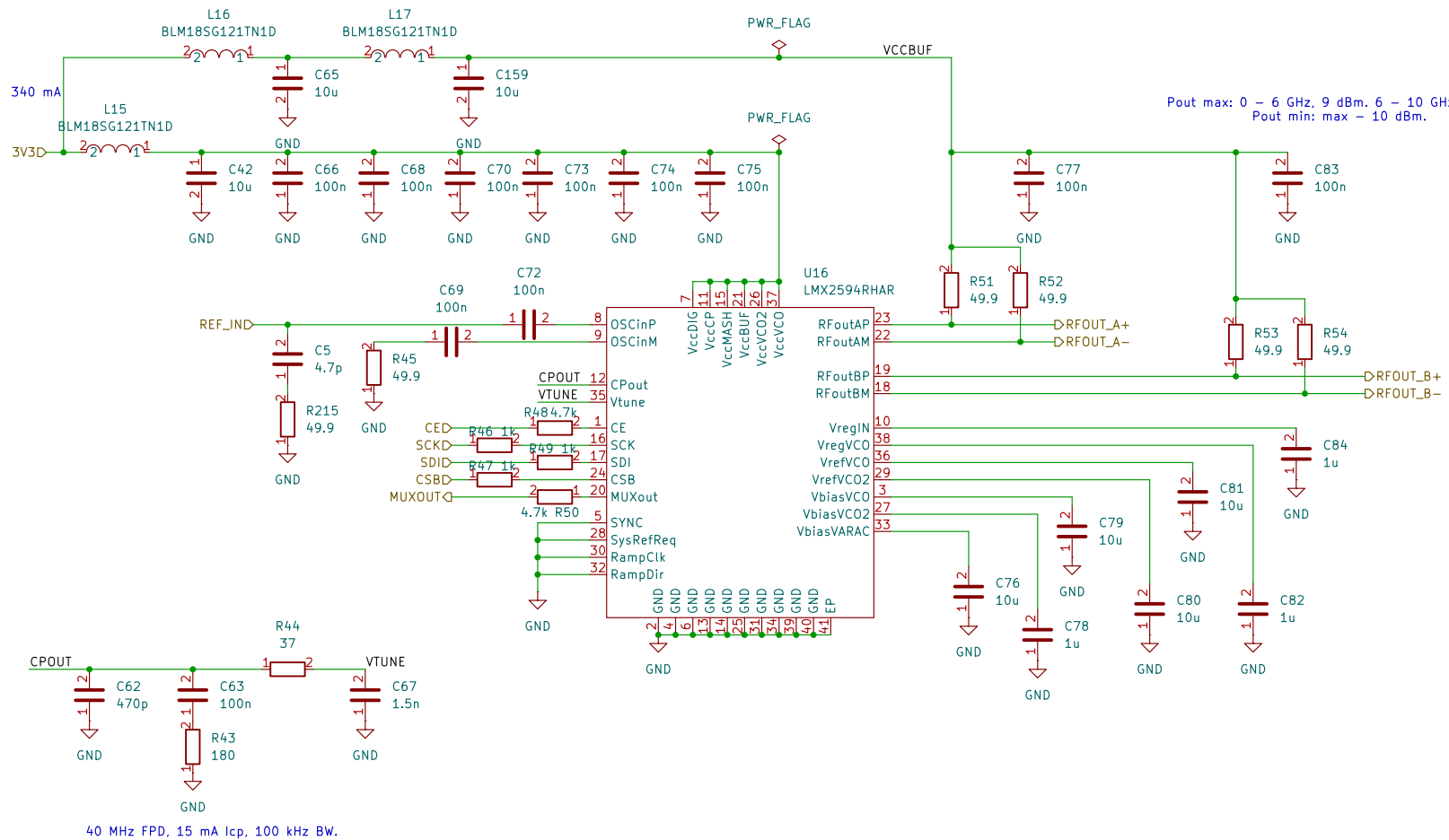
Size: A4

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Sheet: /Source 1/PLL/

File: pll.kicad_sch

Title: PLL

Size: A4

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1

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A

A

FPGA IO1



File: fpga_io1.kicad_sch

FPGA IO2

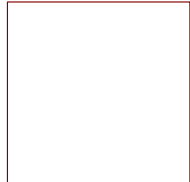


File: fpga_io2.kicad_sch

B

B

FPGA Config



File: fpga_conf.kicad_sch

C

C

D

D

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Sheet: /FPGA/
File: fpga.kicad_sch

Title:

Size: A4

Date: 2025-03-02

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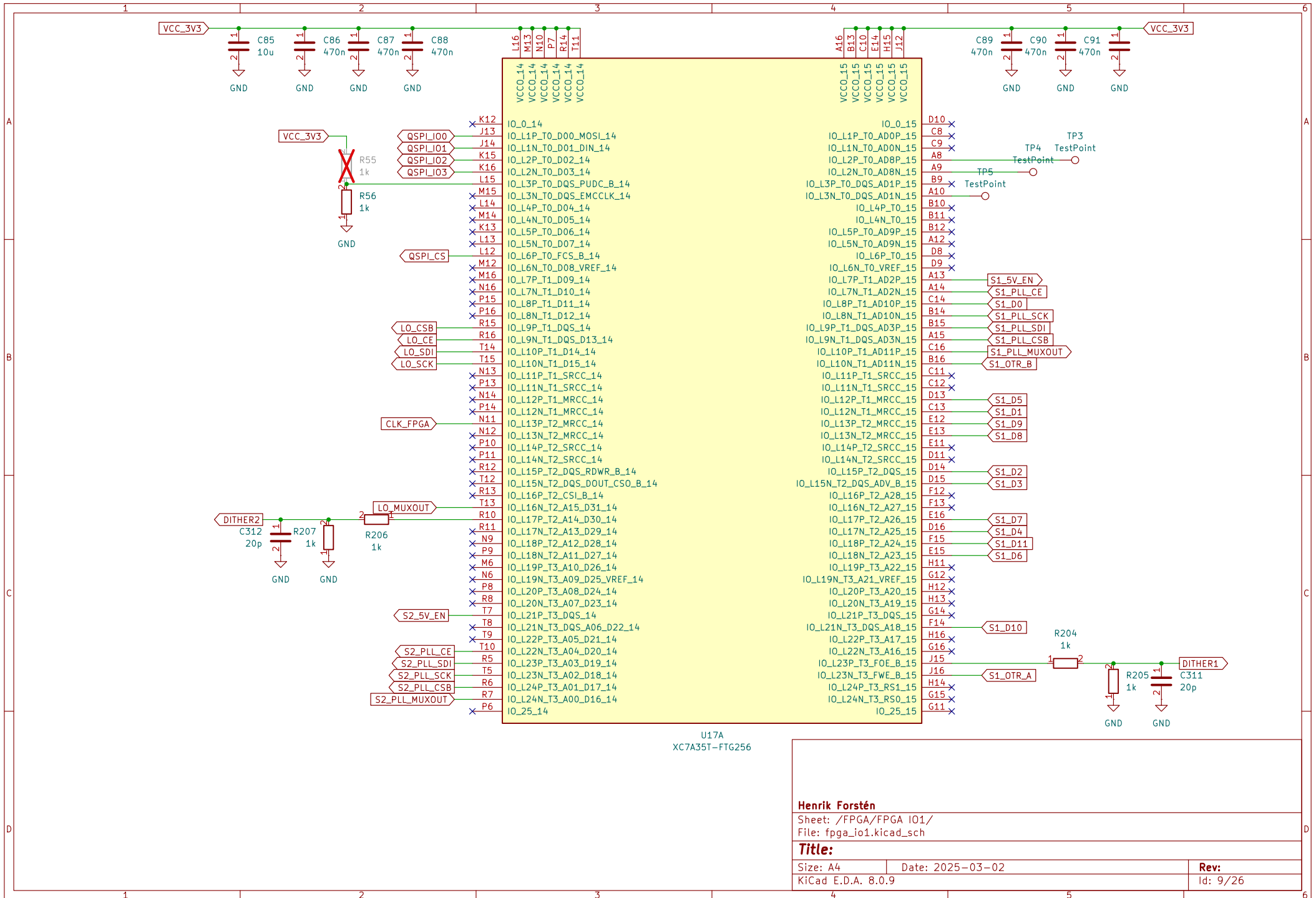
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6



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Sheet: /FPGA/FPGA IO1/
File: fpga_io1.kicad_sch

Title:

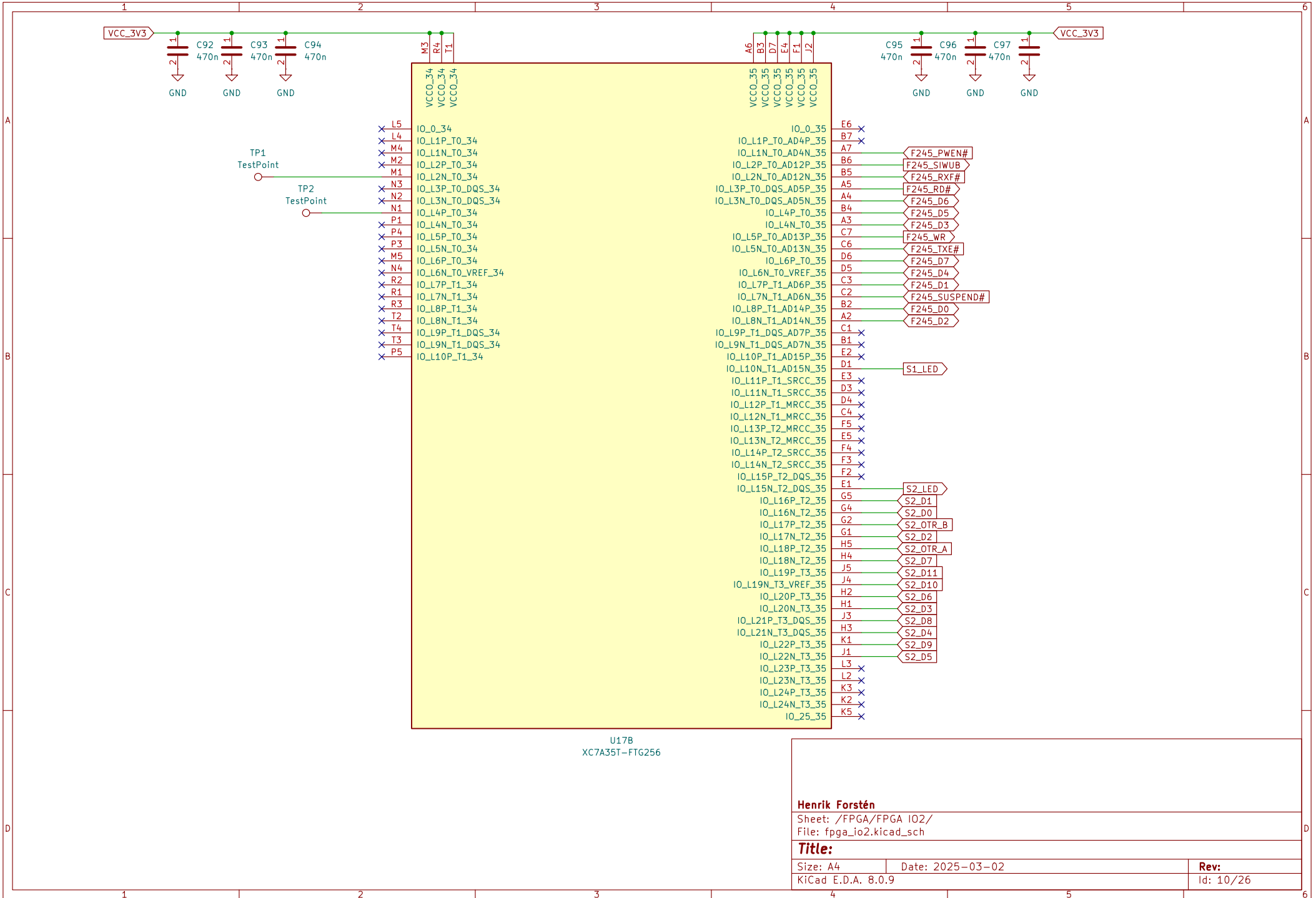
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Date: 2025-03-02

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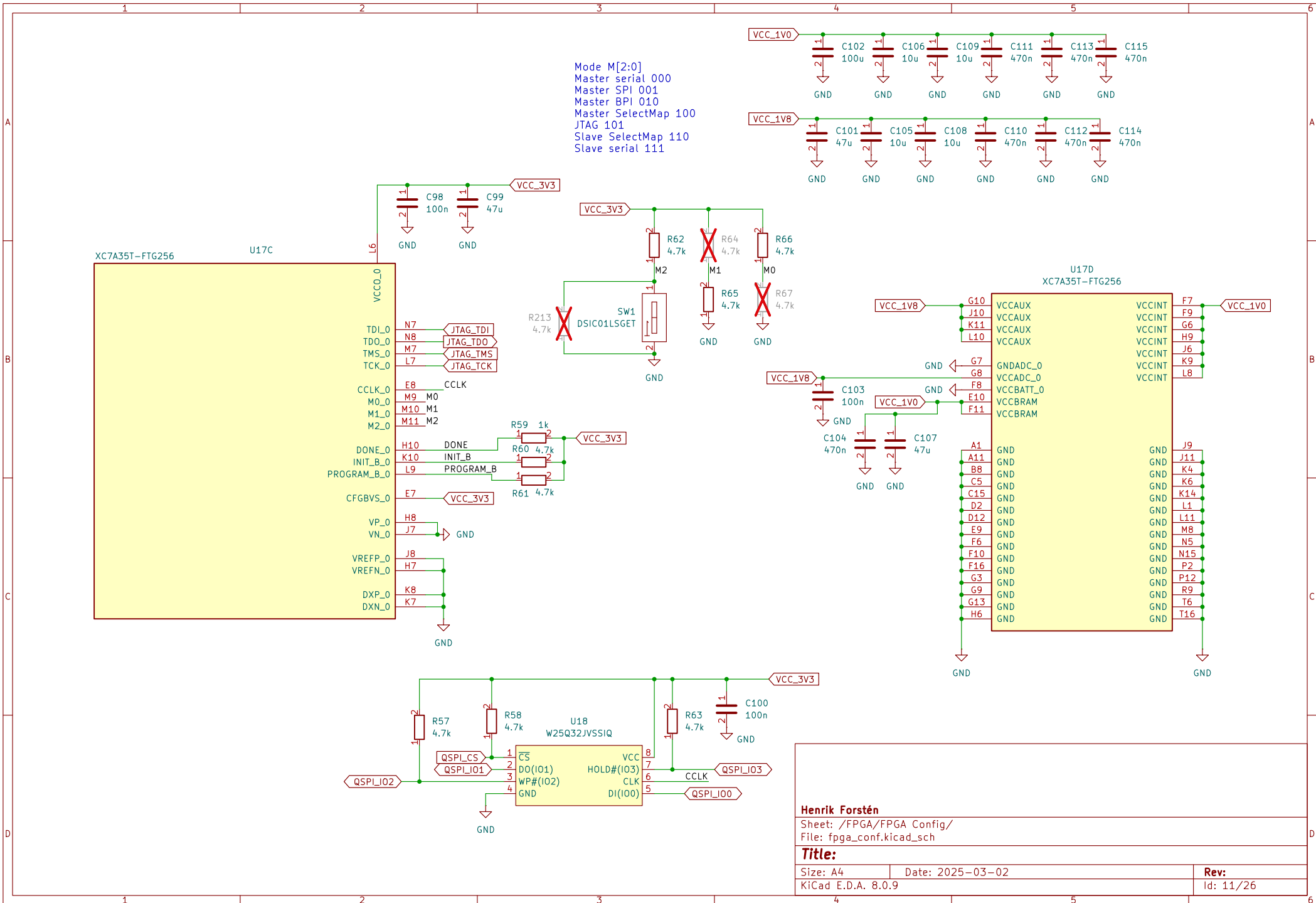
Rev:

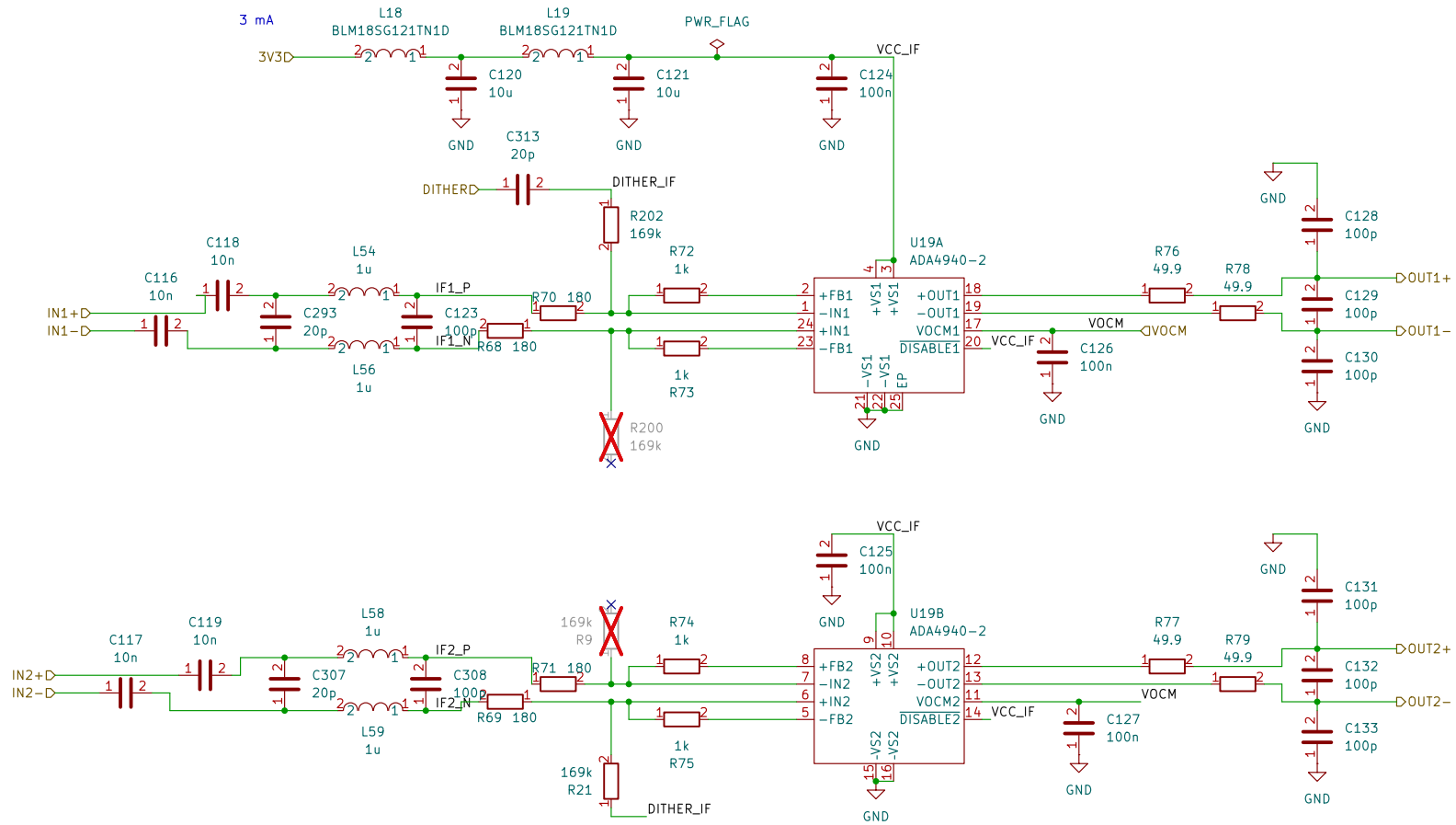
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U17B
XC7A35T-FTG256

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Sheet: /FPGA/FPGA IO2/		
File: fpga_io2.kicad_sch		
Title:		
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Sheet: /Source 1/ADC/IF/
File: if.kicad_sch

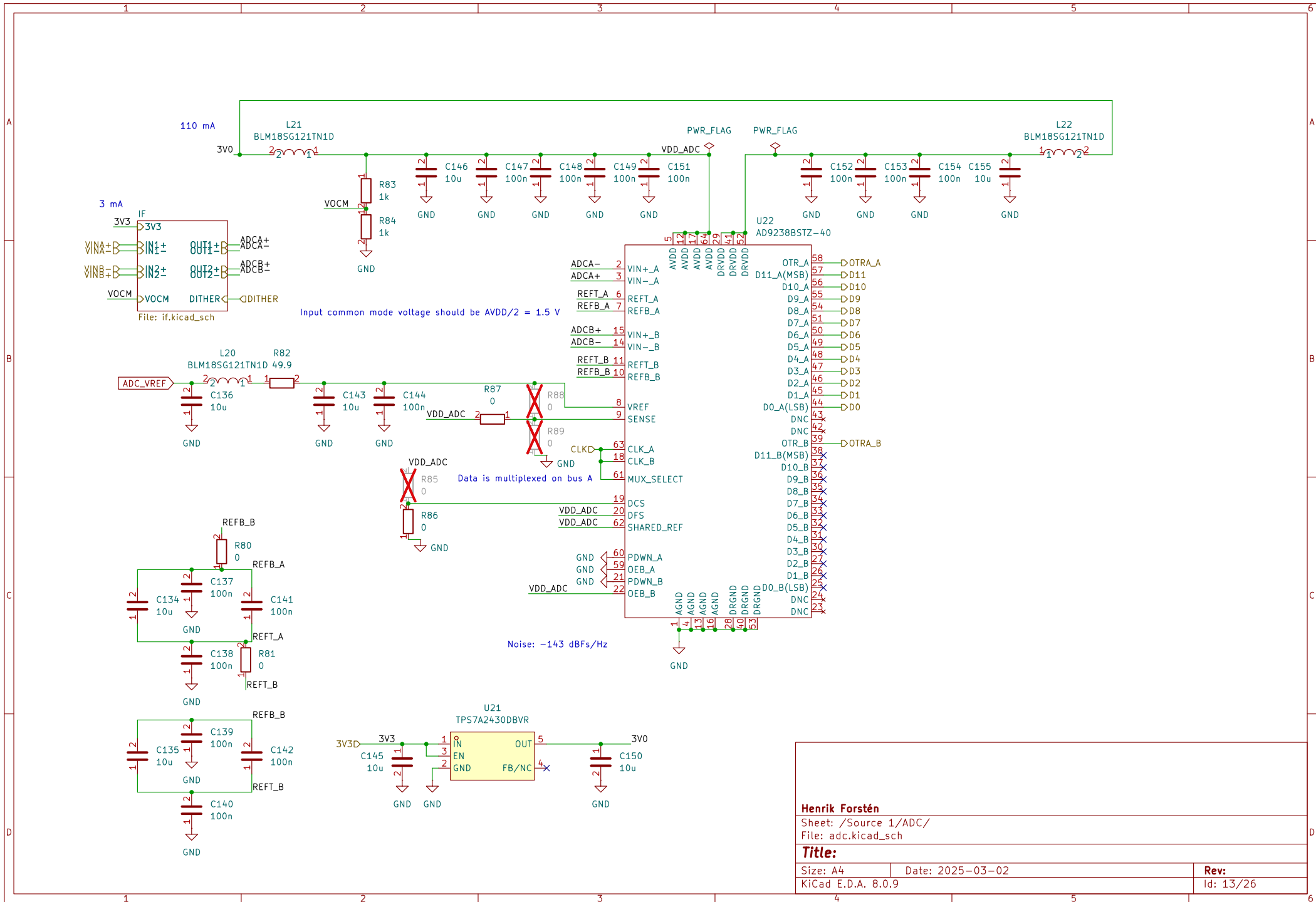
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Size: A4 Date: 2025-03-02

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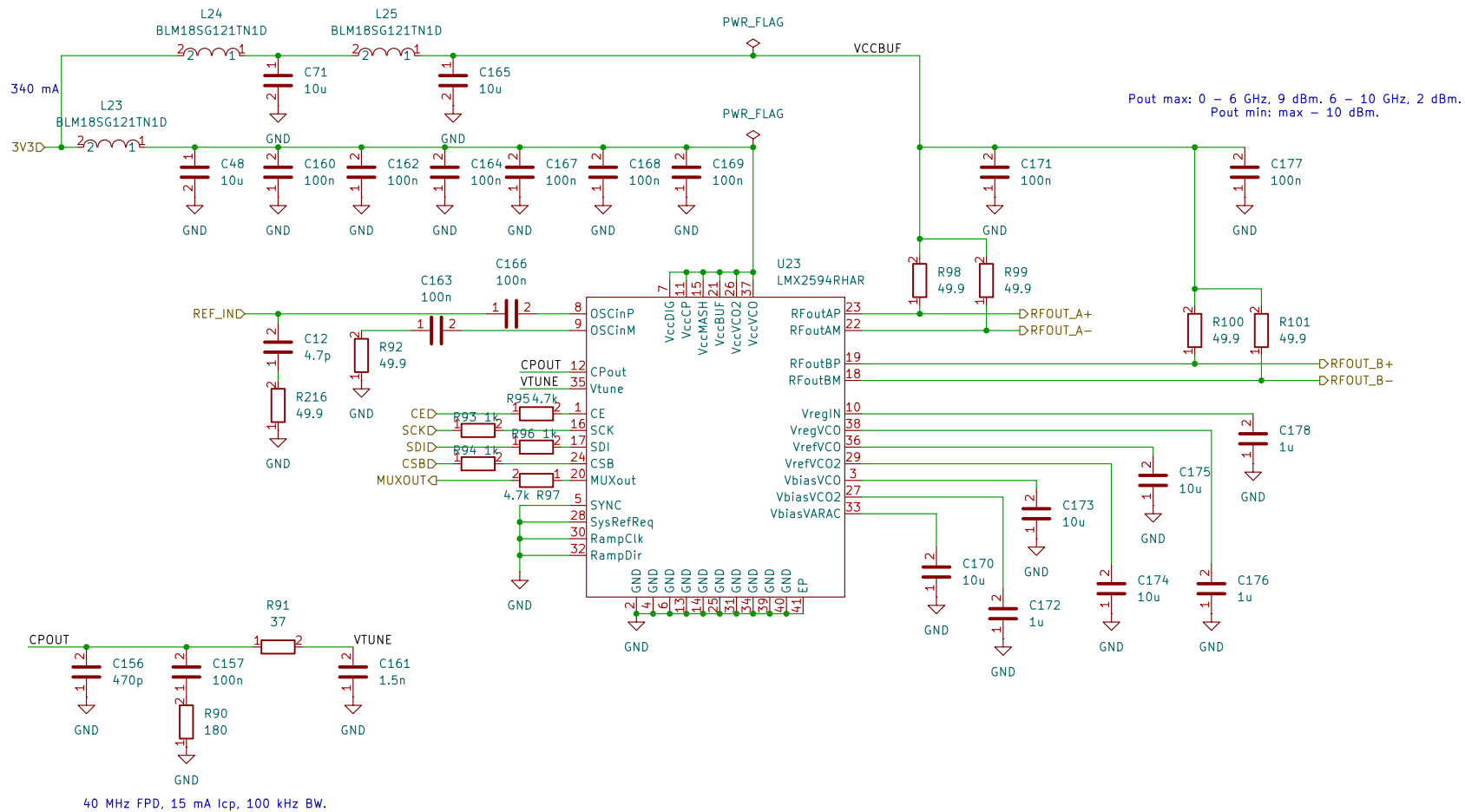
Sheet: /Source 1/ADC/
File: adc.kicad_sch

Title:

Size: A4 Date: 2025-03-02

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Sheet: /Source 2/PLL/

File: pll.kicad_sch

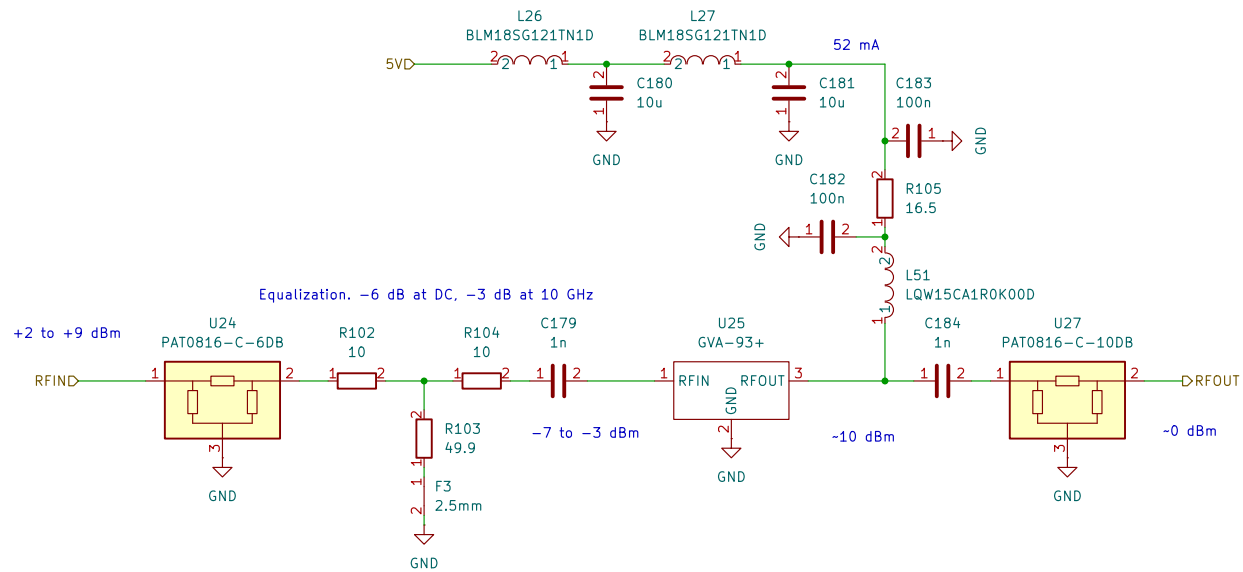
Title: PLL

Size: A4 Date: 2025-03-02

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Rev:

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Equalization, -6 dB at DC, -3 dB at 10 GHz

Source amplifier is added since PLL output matching isn't very good. Source matching is important for VNA operation especially in dual source VNA, where source should terminate the inactive port.

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Sheet: /Source 2/TX amp/
File: tx_amp.kicad_sch

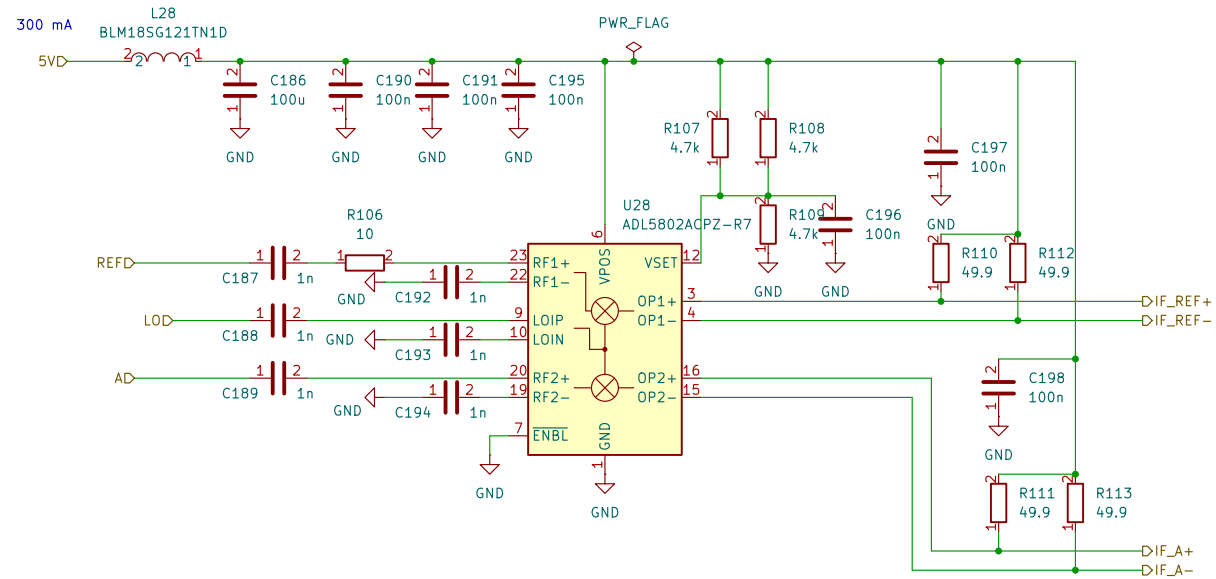
Title: TX amplifier

Size: A4 Date: 2025-03-02

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LO Power: -10 to +10 dBm (0 dBm nominal).
RF Input P1dB: 12 dBm.



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Sheet: /Source 1/Mixer/
File: mixer.kicad_sch

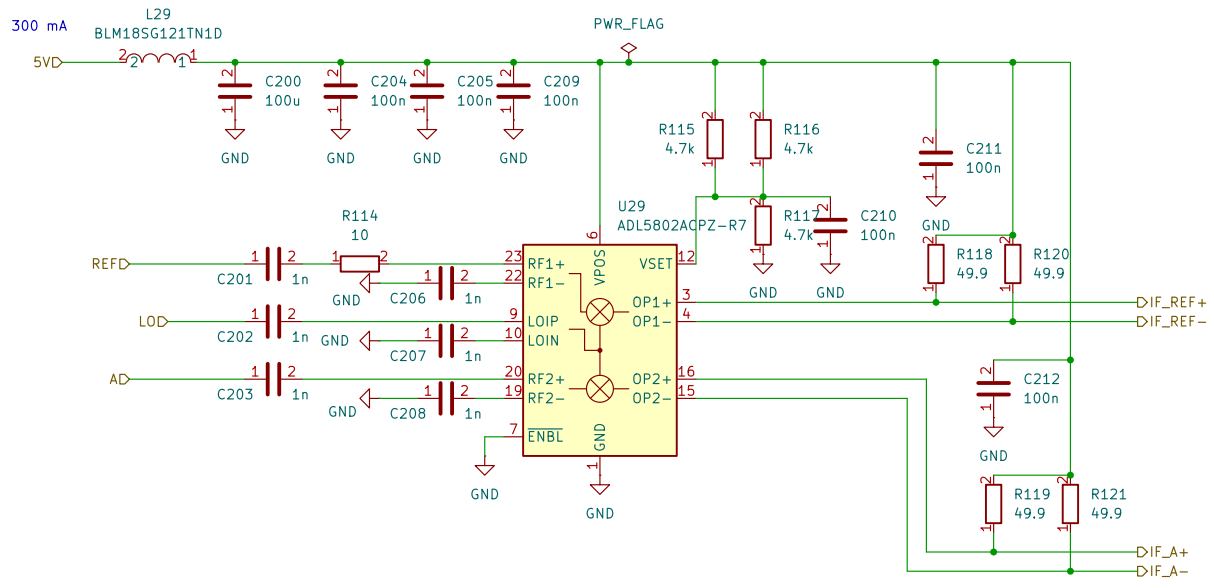
Title: Mixer

Size: A4 Date: 2025-03-02

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Rev:
Id: 16/26

LO Power: -10 to +10 dBm (0 dBm nominal).
RF Input P1dB: 12 dBm.



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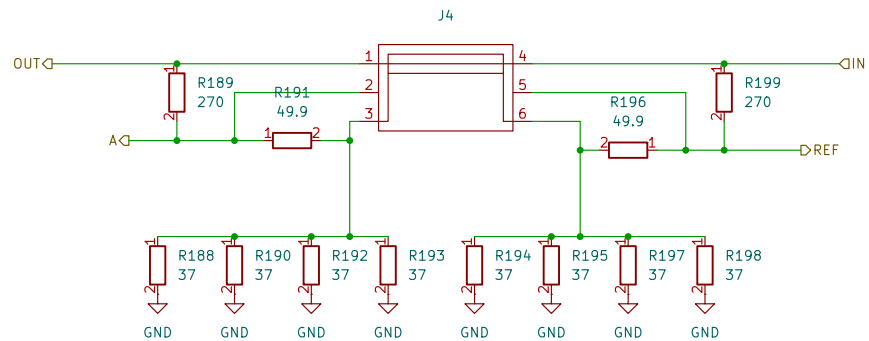
Sheet: /Source 2/Mixer/
File: mixer.kicad_sch

Title: Mixer

Size: A4 Date: 2025-03-02

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Sheet: /Coupler2/
File: coupler.kicad_sch

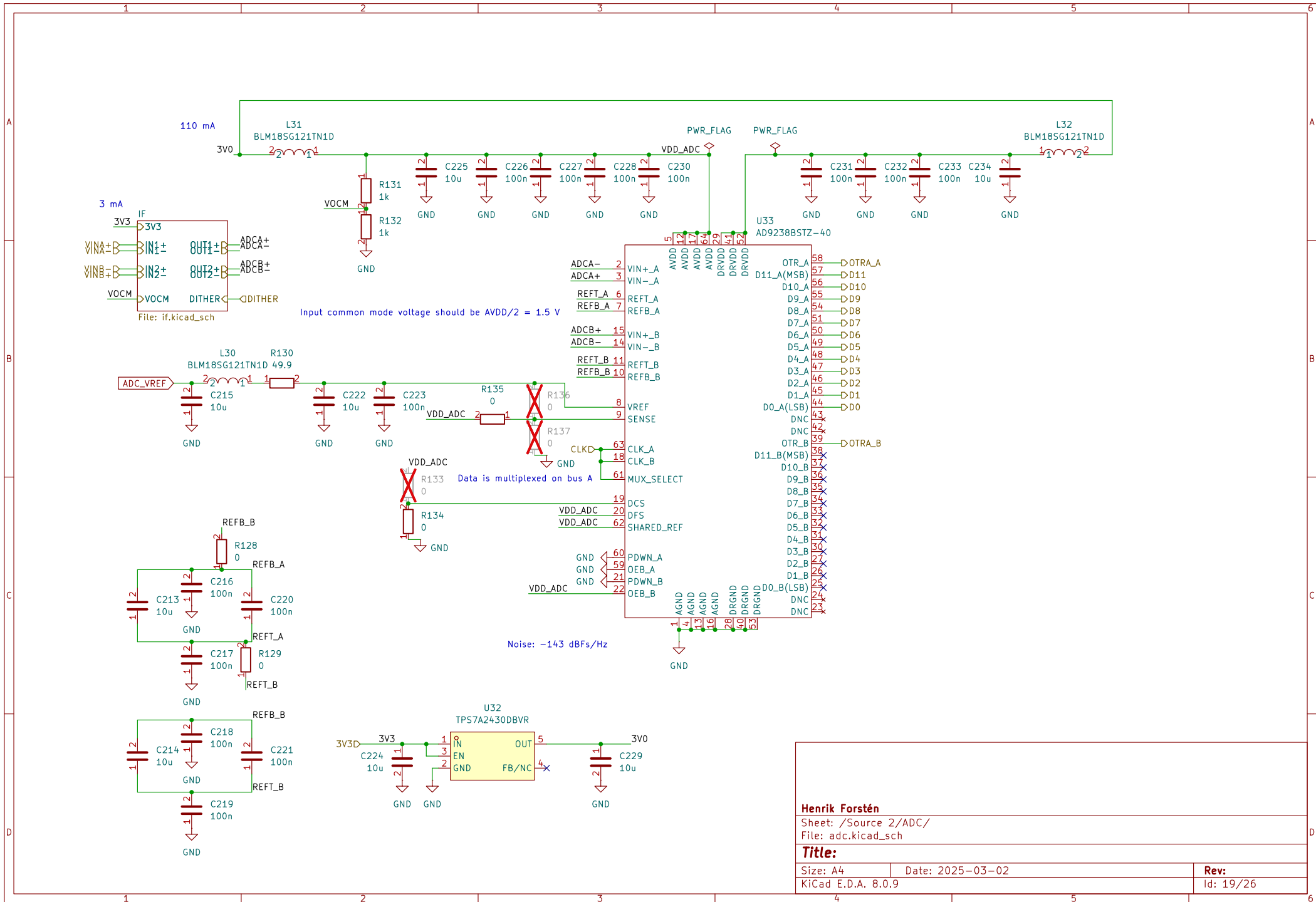
Title: Coupler

Size: A4 Date: 2025-03-02

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Sheet: /Source 2/ADC/
File: adc.kicad_sch

Title:

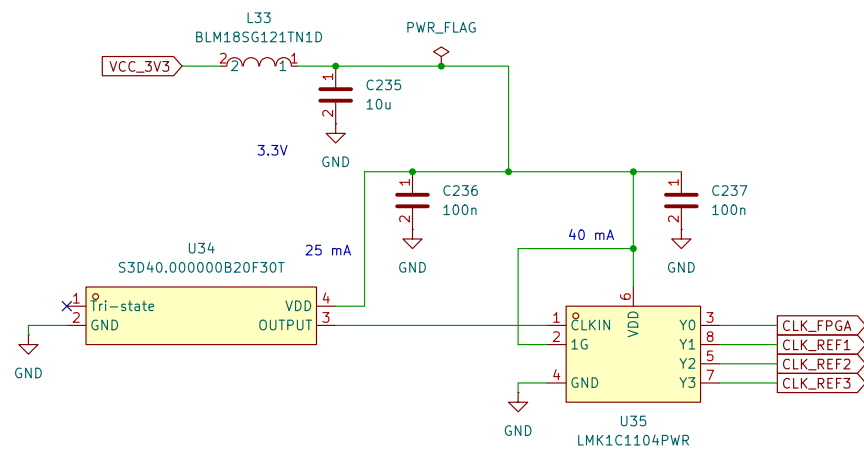
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Date: 2025-03-02

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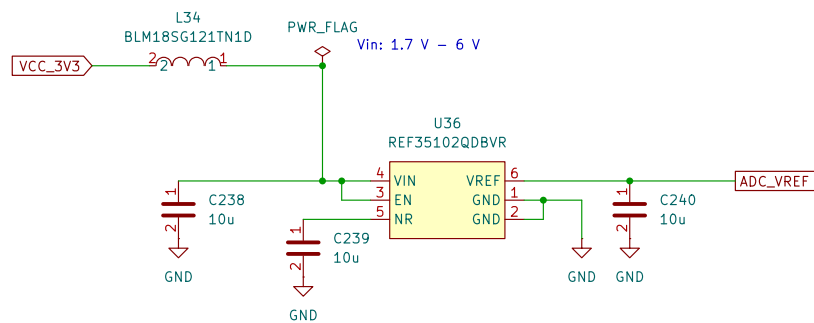
Sheet: /Clock/
File: clock.kicad_sch

Title: Clock

Size: A4 Date: 2025-03-02

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Rev:
Id: 20/26



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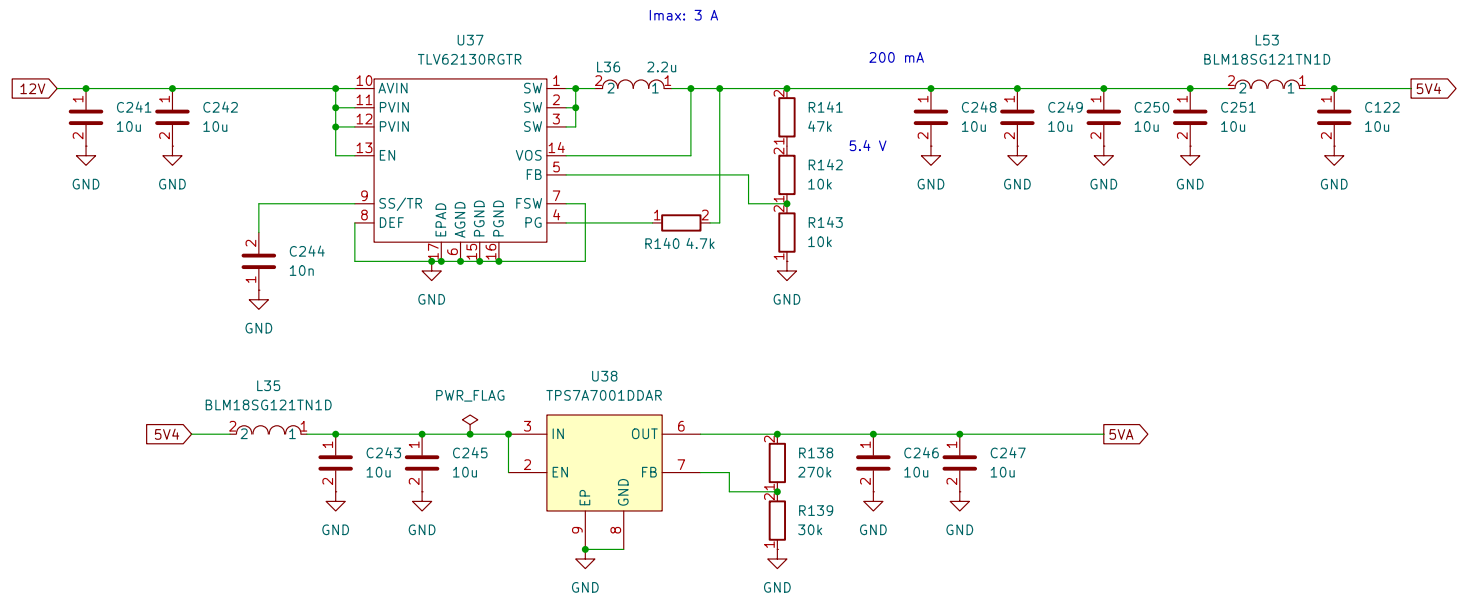
Sheet: /Vref/
File: vref.kicad_sch

Title: Vref

Size: A4 Date: 2025-03-02

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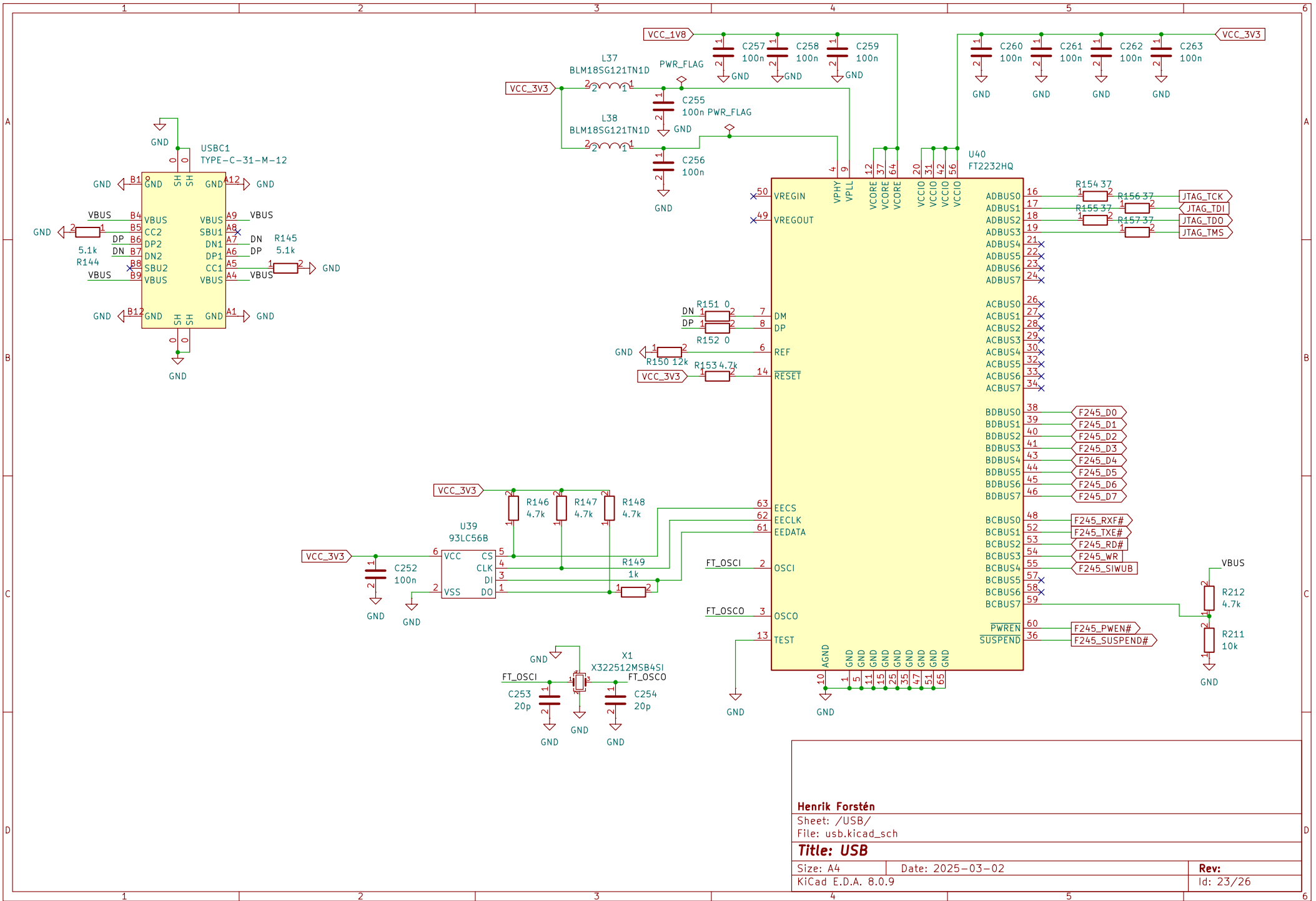
Sheet: /Analog power/
 File: analog_power.kicad_sch

Title: Analog power

Size: A4 Date: 2025-03-02

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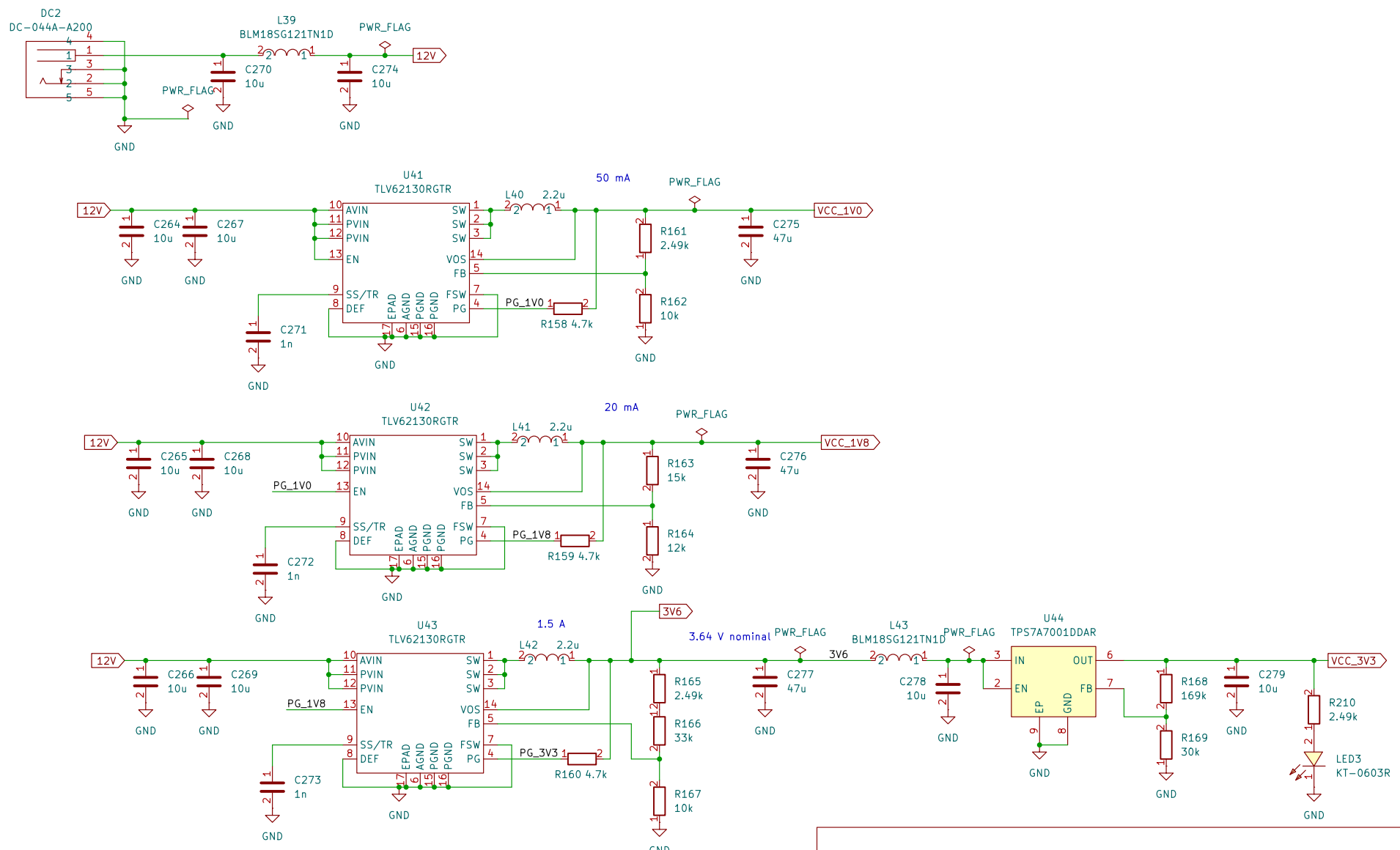
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File: usb.kicad_sch

Title: USB

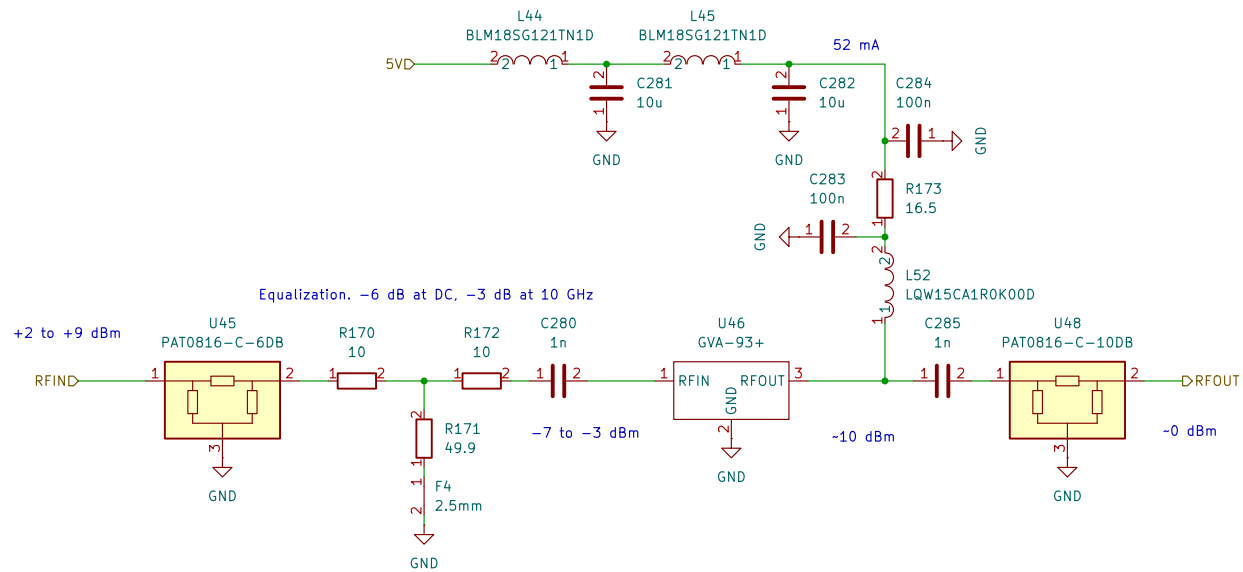
Size: A4 Date: 2025-03-02

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 Sheet: /Digital power/
 File: digital_power.kicad_sch
Title: Digital power
 Size: A4 Date: 2025-03-02
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Source amplifier is added since PLL output matching isn't very good. Source matching is important for VNA operation especially in dual source VNA, where source should terminate the inactive port.

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Sheet: /Source 1/TX amp/
File: tx_amp.kicad_sch

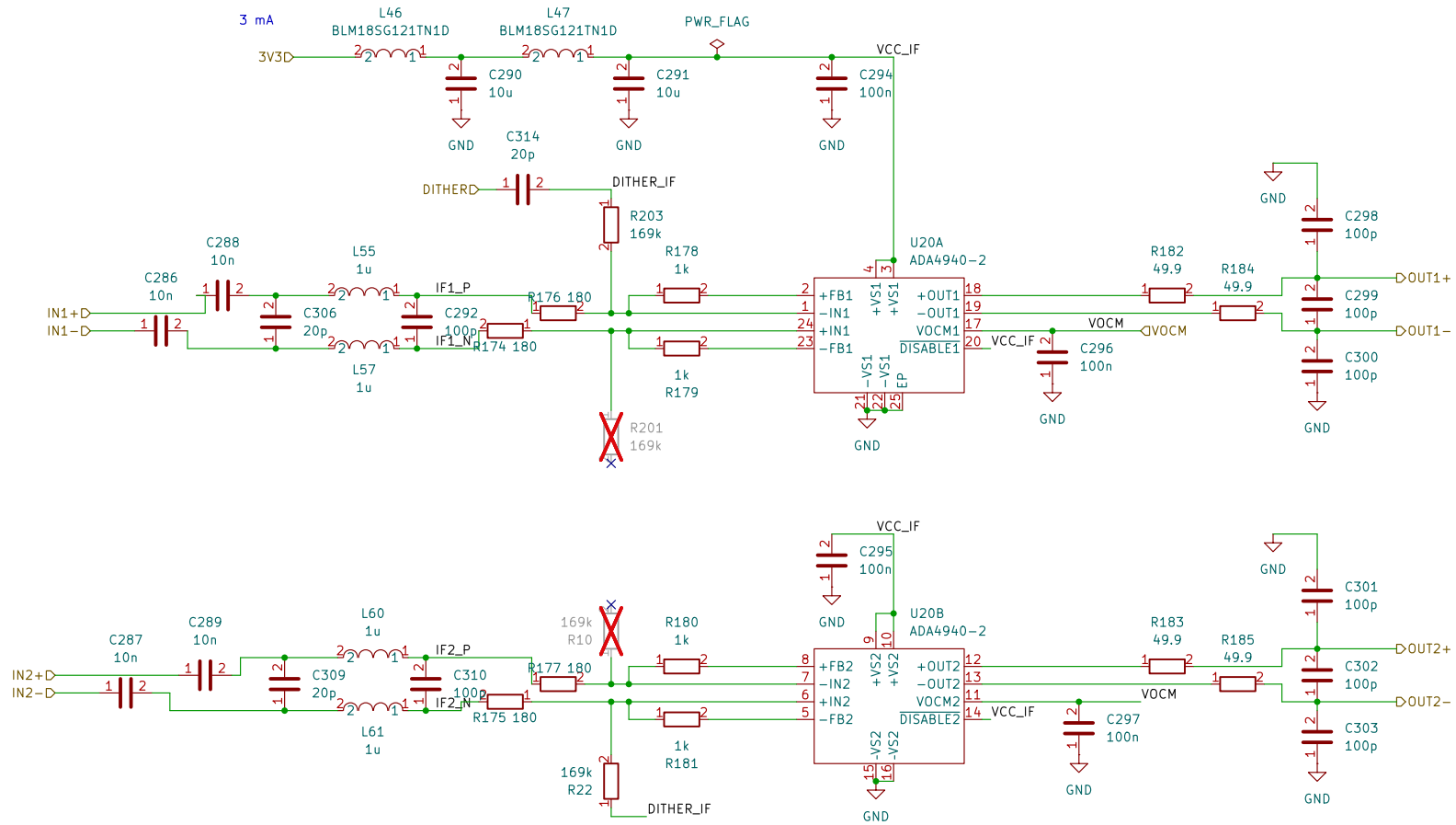
Title: TX amplifier

Size: A4 Date: 2025-03-02

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Sheet: /Source 2/ADC/IF/
File: if.kicad_sch

Title:

Size: A4 Date: 2025-03-02

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